Design of Power and Delay Efficient Carry Select Adder

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Abstract: With the development in the technology, every application is concentrating in high speed and low power requirements. Among the conventional adder structures, Carry Select Adder (CSLA) is said to be a fastest adder. Also to perform fast arithmetic functions, CSLA is mainly used in many data processing processor. This paper provides high speed efficient carry select adder. The adder is designed using CMOS logic. This adder is designed using the tool cadence virtuoso UMC 90nm technology. The carry select adder consists of 4-bit ripple carry adder and an array of 2:1 multiplexers. This adder decreases the power consumption compared to other adder and improves the speed. Here, the performance is analyzed in terms of different parameters. According to the estimation done, the propagation delay and power consumption is reduced.

KEYWORDS: Carry Select Adder, CMOS logic, adder, multiplexer.

I.INTRODUCTION

Adder is mainly used in all electrical applications. In microprocessors, millions of instructions per second are performed. Through the adder, the speed of addition is limited by the time required to propagate a carry in digital adders. In an elementary adder, the sum for each bit position is sequentially generated after the previous bit position has been summed and a carry propagated into the next position.

Computational circuits are based on arithmetic functions which is basic for any arithmetic computation. Designing adders has many ways. RCA contains multiple full adders to add n-bit binary number. In RCA each full adders, C_{in} is the C_{out} of previous full adder i.e., each carry bit ripples to next full adder. RCA's layout is simple but it has larger delay time as each adder waits for carry bit to be calculated from previous full adder. In digital system and in arithmetic functions, addition is mainly used for overall performance.

In many computational systems, to alleviate the problem of carry propagation delay by independently generating multiple carriers and then select a carry to generate the sum CSLA is used. Because of uses of multiple pair of ripple carry adders, CSLA is not area efficient.

CSA's basics is to use block of two ripple carry adder [1] in which one has C_{in}=0 and other has C_{in}=1. These blocks are calculated in parallel. The C_{in} signal for block calculates its resulting C_{out} which propagates to next carry select block. This consumes more time in implementation.

II.BASICS OF CSA

The primary concept is to use three one bit full adder and two bit multiplexer for adding two bits. Here, one full adder adds the MSB with the assumption of C_{in} as 0 for one adder and 1 for other adders [2] . Based on the carry produced by adder for LSB, multiplexer chooses output from one of other adders. Using multiplexers has greater advantages in speed as the multiplexer are faster than adder.

Cascading is possible in CSA using longer ripple carry adder and the lengthy sequence is based on speed of adders and multiplexers. Generally, CSA adders consist of ripple carry adder and multiplexers in which RCA's is cascade one bit full adders. Delay of CSA is a delay of full adder and multiplexer. In CSA, power dissipations is high which has to be overcome.

III.LITERATURE SURVEY

Though there are many adders designed for several purposes, satisfying every needs by designing an adder without any disadvantages is difficult. Here, designing adder which is best in low power consumption and fast performance is challenging. CSA provides a compromising solution compared to RCA and CLA. There are many CSA approaches available in which most of them use RCA.

T.Y.Chang and M.J. hsloa [3] suggested a carry select adder scheme in with replacement of one ripple carry adder with add one circuit, instead of dual ripple adder. This is because one ripple carry requires 29.2% fewer transistors and speed penalty 5.9% for bit length n=64. Considering speed factor as important two carry select adder blocks could be substituted in proposed scheme.

Damarla paradhasarathi and Prof. K.Anusudha [4] proposed an area efficient Carry Select Adder by using Common Boolean Logic. The correct output is selected according to the logic states of the carry in signal through the multiplexer. The proposed architecture reduced the area and delay compared to SQRT CSLA.

B.Ramkumar(2012), H.M.Kittur and P.M.Kannan [5] suggested an approach for speeding of addition. 16, 32 and 64 bit adder architecture was compared with conventional adder. In conventional adders parallel multipliers are used for speed of final additions. CLA arranged in CSA form was used. But this occupies more chip area due to multiple pair of RCA in generation of partial sum and carry using C_{in}=0 and C_{in}=1. To remove the complexity they replaced RCA with C_{in}=1 with BEC logic. This in turn reduced the area and delay in adder structure.

IV. IMPLEMENTATION OF 8 BIT CARRY SELECT ADDER

4.1 8 BIT CARRY SELECT ADDER

The implementation of 8 bit carry select adder is shown in Figure 1. Here, the adder is separated into two 4 bit groups [6]. The lower order bits as a3 a2 a1 a0 and b3 b2 b1 b0 are given into the 4 bit adder L to produce the sum bits s3 s2 s1 s0 and a carry out bit c4. The higher order a7 a6 a5 a4 which are used as inputs to two 4 bit adders.

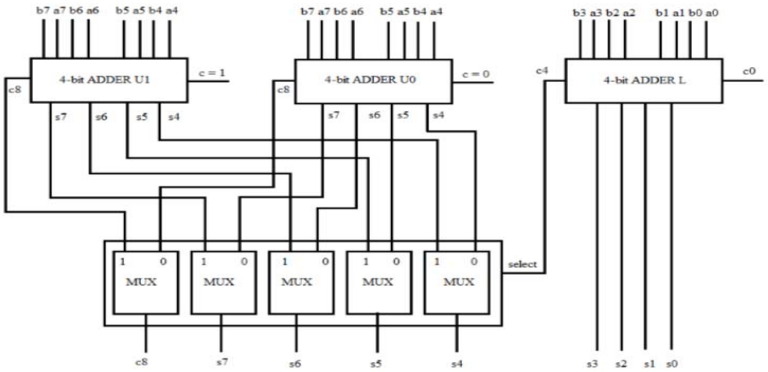

Figure 1: Implementation 8 bit CSA

The sum with C_{in}=0 is calculated by the adder U0 where U1 calculates with C_{in}=1. Then the result from both set is given as an input to multiplexers. The carry from c4 of adder L is used as the selection signal for multiplexer. When c4=0, the U0 result is sent to the output. When c4=1, selects the result of U1 as s7 s6 s5 s4. The multiplexer which also selects the carry out bit c8.

V. SCHEMATIC SIMULATION

The transistor level diagram of CSA is implemented using cadence virtuoso UMC 90nm technology. The instances of each individual block is combined together to form the complete CSA circuit [7]. Initially, the adder circuit is designed using 8T and 10T cell. Then the output is simulated for both the adder circuits. The power and delay of both the adder is calculated and compared. From the comparison the optimal adder is selected. From the optimized adder, Carry Select Adder is simulated.

5.1. 4-BIT FULL ADDER USING 8T AND 10T

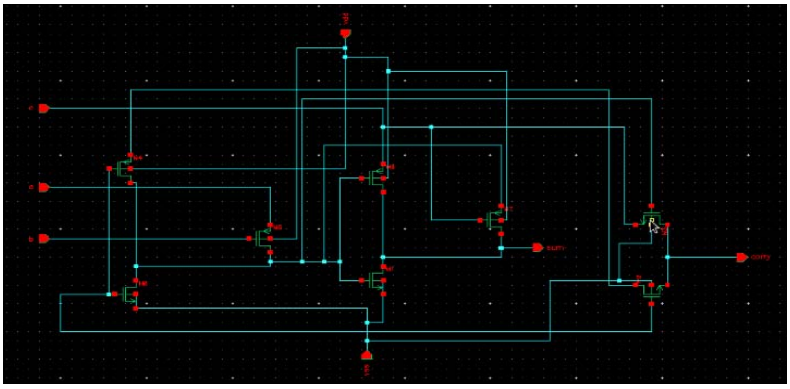

Figure 2: schematic of full adder using 8T

Figure 3: schematic of full adder using 10T

5.2. 2:1 MULTIPLEXER

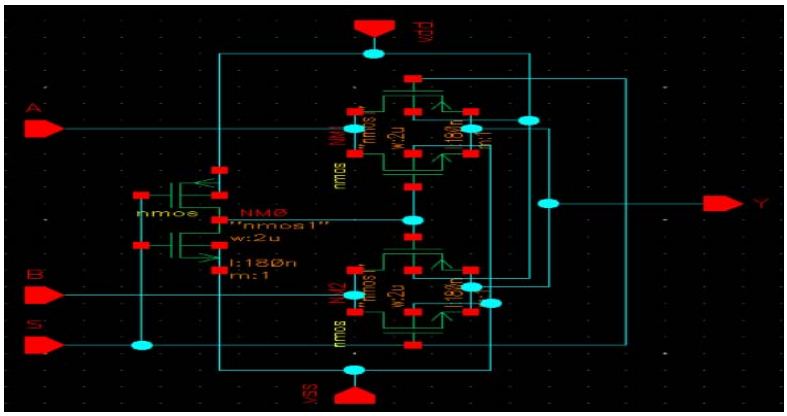

Figure 4: schematic of 2:1 multiplexer

5.3. RIPPLE CARRY ADDER

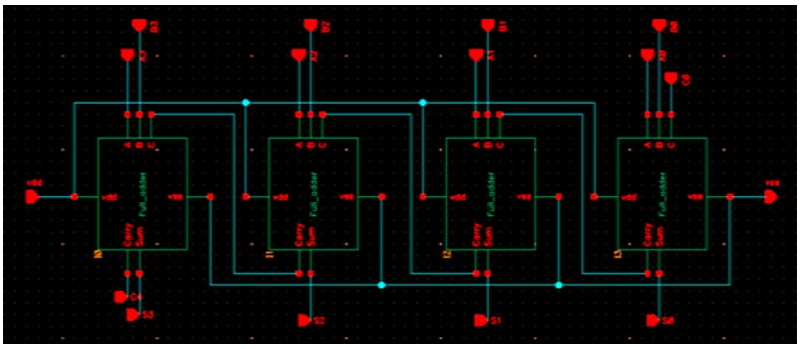

Figure 5: schematic of Ripple Carry Adder

5.4. 8 BIT CARRY SELECT ADDER

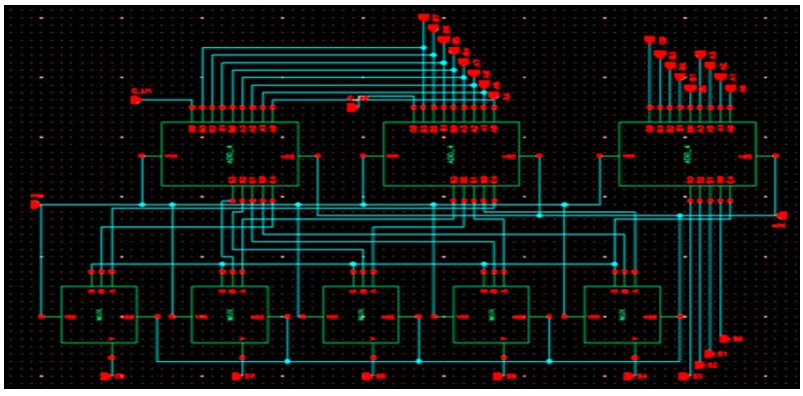

Figure 6: schematic of 8 bit CSA

VI. SIMULATION RESULTS

The 8 bit Carry Select Adder is simulated with the supply voltage of 1.5V. Figure 6 which shows the complete implementation of Carry Select Adder.

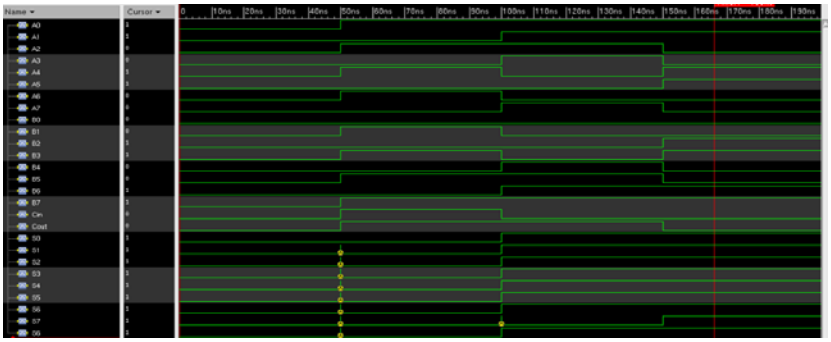

Figure 7: simulation result of 8 bit CSA

The performance analysis of 8T and 10T Full Adder is compared in terms of power and delay.

Table 1. Performance Analysis of 8T and 10T full adder

S.NO	PARAMETERS	8T FULL ADDER	10T FULL ADDER
1	NO OF TRANSISTOR	8	10
2	POWER(W)	4.40E-10	6.10E-11
3	DELAY(ns)	SUM=8.86E-11 CARRY=1.25E-10	SUM=1.02E-10 CARRY=9.87E-11

From the comparison Table 1, it is known that 10T full adder is the optimal one. The Carry Select Adder is proceeded further using the 10T Full Adder. Then the analysis of CSA is performed after the complete implementation.

No.Of.Transistors :190

Power(uW) :11.77

Delay(ps) :310

VII. CONCLUSION

Here, the 8 bit Carry Select Adder is presented which overcomes the certain feedback. This adder is designed using 90nm CMOS process technology. This carry select adder efficiently overcomes the drawback by reducing the computational time and improves the speed. The performances are analyzed in terms of transistor count, power and delay.

REFERENCES

[1] Yi Wei,Ji-zhong Shen, " Design of a novel low power 8 transistor 1-bit full adder cell", *Journal of Zheijiang university* .,vol 12, issue 7,pp 604-607, 2011

[2] R. Hasmain, "A new design for high speed and high density carry select adders". *Proceedings of IEEE Midwest symp. On circuits and systems*.pp.1300-1303,2000.

[3] T.Y. Chang and M.J.Hsiao, "Carry Select Adder using single ripple carry adder", *Electronics letters*, vol.34 n0 22 pp,2101-2103, 1998.

[4] Damarla Paradhasaradhi, prof.K.Anusudha "An area efficient enhanced SQRT carry select adder", D paradhasaradhi et al int. *Journal of Engineering Research and Applications* ISSN:2248-9622 vol.3, issue 6, pp.876-880, 2013.

[5] B.Ramkumar, H.M.Kiitur and P.M.Kannan, "ASIC implementation of modified faster carry select adder", *Eur.J.Sci.Res.*,vol.42, no.1, pp.53-58,2010.

[6] Sarabdeep Singh and Dilip Kumar, " Design of area and efficient modified carry select adder" , *International Journal of Computer Applications*(0975-8887) vol.33 no.3, 2011.

[7] Dan Wang, Maofeng Yang, Wu Cheng Xuguang, Zhangming Zhu, Yintang Yang "Novel Low power full adder cells in 90nm CMOS technology", IEEE conference on industrial Electronics and Application, pp.430-433,2009.